CURRICULUM VITAE (2016)

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Date of Birth: 12-4-1956

RESEARCH/TEACHING INTERESTS

Computer Arithmetic, Computer Architecture and Organization, Design and Testing of Digital Systems, Embedded Open Software/Hardware Development Systems, Telecommunications and Computer Networks, Microprocessors/Microcontrollers.

DEGREES

PhD in Computer Science, University of Thessaloniki, 1985
MSc in Electronics and Computer Engineering, University of Athens, 1982
BSc in Physics, University of Athens, 1979

PROFESSIONAL/RESEARCH EXPERIENCE

5/1994→today : Professor, Department of Informatics, TEI of Athens.
November 2015 → today, Director of the Laboratory of Computer Engineering.

12/1988-5/1994 : Computer and Telecommunication System Engineer, Department of Teleinformatics, Hellenic Telecommunication Organization (OTE).
Adjunct Instructor, Dept. of Computer Engineering, TEI of Piraeus.

8/1987-12/1988 : Computer Engineer, Dept. of Informatics Development, Ministry of the Presidency of the Government.
Adjunct Instructor, Dept. of Computer Engineering, TEI of Piraeus.

4/1986-8/1987 : Adjunct Instructor, Dept. of Computer Engineering, TEI of Piraeus

6/1984-3/1986 : Research Assistant, Digital Systems and Microprocessors Lab, Research Center of the Hellenic Air Force (HAF).

4/1983-4/1984 : Research Assistant, Digital Systems Lab, Physics Department, University of Thessaloniki.

3/1979-3/1983 : Research Assistant, Digital Systems Lab, National Research Center of Physical Sciences "Democritos", Athens.

TEACHING EXPERIENCE

I. Graduate level

3/2012-today. Supervisor of PhD thesis in collaboration with the Department of Electrical and Computer Engineering of the National Technical University of Athens.

10/2013-today. Master Program in "Informatics and Multimedia System" offered by TEI of Athens in collaboration with University of Limoges, France.
Courses taught:
1. Advanced Computer Architectures
2. Computer Networks
3. Supervisor of Master Thesis

10/2000-7/03. Master Program in "Telematics Management" offered by TEI of Piraeus in collaboration with Danube University of Krems, Austria.
Courses taught:
1. Computer Technology
2. Telecommunication Networks
3. Supervisor of Master Thesis

II. Undergraduate level

5/1994→today : Undergraduate program, Dept. of Informatics, TEI of Athens.
Courses taught:
1. Computer Organization and Design
2. Digital Systems

9/1984→7/95 : Undergraduate program, Dept. of Computer Engineering, TEI of Piraeus.
Courses taught:
1. Microprocessor Systems
2. Digital Systems

2004-2010: Undergraduate program, Dept. of Informatics, Open University of Greece
Course taught
Digital Systems, Computer Architecture and Microprocessors

ADMINISTRATIVE POSITIONS

1. Vice President of the Department of Informatics.

2. Founder and head of the Sector of Computer and Communication Systems Technology of the department of Informatics.

INTERNATIONAL CONFERENCE ORGANIZING COMMITTEE MEMBER

1. Program Committee member of the IEEE Computer Society Annual Symposium on VLSI (IS VLSI), Kefalonia, Greece, 2010.
2. Program Chair of the IEEE International Conference on Design & Technology of Integrated Systems in the Nanoscale Era, (DTIS), Athens, Greece, 2011.
3. Program Committee of the IEEE International Conference on Design & Technology of Integrated Systems in the Nanoscale Era, (DTIS), Tunis, 2012
4. Program Committee of the IEEE International Conference on Design & Technology of Integrated Systems in the Nanoscale Era, (DTIS), Athens, 2014
5. Program Committee of the IEEE International Conference on Design & Technology of Integrated Systems in the Nanoscale Era, (DTIS), Italy, 2015
6. Program Committee of the IEEE International Conference on Design & Technology of Integrated Systems in the Nanoscale Era, (DTIS), Turkey, 2016

RESEARCH PROJECTS

1. "VLSI design of high reliability digital circuits", TEI of Athens, Internal Research Project, 2000-2001, Research Coordinator.

2. "VLSI design and fault testing of residue number system (RNS) based functional units based on for Digital Signal Processors (DSP) and cryptography systems" European Community and Greek Government Project Archimedes II, 2005-2007, Research Coordinator.

3. "Design and implementation of efficient arithmetic units for non conventional number systems", European Community and Greek Government Project Archimedes III, 2012-15, Research Coordinator.

4. "Photonic networks based on photonic integrated circuits", European Community and Greek Government Project Archimedes III, 2012-15.

PUBLICATIONS

A. International Patents

1. "High-Speed Regular-Layout Modulo 2^n-1 Adders", L. Kalampoukas, D. Nikolos, C. Efstathiou, H. T. Vergos, J. Kalamatianos, World Patent # WO0208885.

B1. International Journals

1 C. Efstathiou, C. Halatsis, "Efficient modular design of m-out-of-2m TSC checkers, for m = 2^k-1, k > 2", Electronics Letters, vol. 21, no. 23, pp.1083-84, Nov. 1985.

2 C. Efstathiou, "Efficient MOS implementation of totally self-checking two-rail code checkers", International Journal of Electronics, vol. 68, no. 2, pp. 259-264, Feb. 1990.

3 A. Paschalis, C. Efstathiou, C. Halatsis, "An efficient TSC 1-out-of-3 code checker", IEEE Transactions on Computers, vol. 39, no. 3, pp. 407-411, March 1990.

4 C. Efstathiou, D. Nikolos, J. Kalamatianos, "Area-Time efficient modulo 2^n-1 adder design", IEEE Transactions on Circuits and Systems-II, vol. 41, no. 7, pp. 463-467, July 1994.

5 L. Kalamboukas, D. Nikolos, C. Efstathiou, H. T. Vergos, J. Kalamatianos, "High-Speed Regular-Layout Modulo 2^n-1 Adders", IEEE Transactions on Computers, Special Issue on Computer Arithmetic, vol. 49, no. 7, pp. 673-680, July 2000.

6 H. T. Vergos, C. Efstathiou, D. Nikolos, "Diminished-One Modulo 2^n+1 Adder Design", IEEE Transaction on Computers, vol. 52, no. 12, pp. 1389-1399, December 2002.

7 C. Efstathiou, H. T. Vergos, and D. Nikolos**,** "Handling zero in diminished-one modulo 2^n+1 adders", International Journal of Electronics, vol. 90, no. 2, pp. 133-144, Feb. 2003.

8 Th. Haniotakis, Y. Tsiatouhas, C. Efstathiou, D. Nikolos, "Domino-CMOS Strongly Code-Disjoint and Strongly Fault-Secure 2-out-of-3 and 1-out-of-3 Code Checkers", International Journal of Electronics, vol. 90, no. 2, pp. 145-158, Feb. 2003.

9 H. T. Vergos, and D. Nikolos**,** C. Efstathiou, "Deterministic BIST for RNS Adders", IEEE Transaction on Computers, vol. 52, no. 7, pp. 896-906, July 2003.

10 C. Efstathiou, H. T. Vergos, and D. Nikolos, "Modulo 2^n+1 Adder Design Using Select-Prefix Blocks", IEEE Transaction on Computers, vol. 52, no. 11, pp. 1399- 1406, Nov. 2003.

11 C. Efstathiou, H. T. Vergos, and D. Nikolos, "Modulo 2^n-1 Modified Booth Multipliers", IEEE Transactions on Computers, vol. 53, no. 3, pp. 370-374, March 2004.

12 C. Efstathiou, H. T. Vergos, and D. Nikolos, "Fast parallel-prefix modulo 2^n+1 adders", IEEE Transactions on Computers, pp. 1211-1216, vol. 53, no. 9, September 2004.

13 C. Efstathiou, H. T. Vergos, G. Dimitrakopoulos, and D. Nikolos, "Efficient Diminished-1 Modulo 2^n+1 Multipliers", IEEE Transactions on Computers, pp. Oct. 2005.

14 H. T. Vergos, C. Efstathiou, "Diminished-1 Modulo 2^n+1 squarer design", IEE Proceedings on Computers and Digital Techniques, vol.152, no. 5, pp. 561-566, Oct. 2005.
15 H. T. Vergos, and C. Efstathiou, "On the Design of Efficient Modular Adders", Journal of Circuits, Systems and Computers, vol. 14, no. 5, pp. 965-972, Oct. 2005.
16 N. Sklavos, K. Touliou, and C. Efstathiou, "Security & Privacy Architectural Modules: On the Hardware & Software Integration Platforms", WSEAS Transactions on Information Science and Applications, vol. 3, no 5, pp. 965-971, May 2006.
17 H. T. Vergos, and C. Efstathiou, "On the Design of Efficient Modulo 2^n+1 Multipliers", IET Proceedings on Computers and Digital Techniques, vol. 1, no. 1, pp. 49-57, Jan. 2007.
18 Th. Haniotakis, Y. Tsiatouhas, D. Nikolos, C. Efstathiou, "Testable Designs of Multiple Precharged Domino Circuits", IEEE Transaction on VLSI, vol. 15, no. 4, pp. 461-465, April 2007.
19 H. T. Vergos, C. Efstathiou, "Unifying Approach for Weighted and Diminished-1 Modulo 2^n+1 Adders", IEEE Transactions on Circuits and Systems-II, vol. 55, no. 10, pp. 1041–1045, October 2008.
20 H. T. Vergos, C. Efstathiou, "Efficient Modulo 2^n+1 Adder Architectures", Integration, the VLSI Journal, vol. 42, no. 2, pp. 149–157, February 2009.
21 H. T. Vergos, D. Bakalis and C. Efstathiou, "Fast Modulo 2^n+1 Multi-Operand Adders and Residue Generators", Integration, the VLSI Journal, vol. 43, no. 1, pp. 42–48, January 2010.
22 A. Bogris, D. Syvridis, and C. Efstathiou, "Noise Properties of Degenerate Dual Pump Phase Sensitive Amplifiers", IEEE Journal of Lightwave Technology, vol. 28, no. 8, pp. 1209-1217, April 2010.
23 I. Voyiatzis, C. Efstathiou, "An Efficient Architecture for Accumulator-Based Test Generation of SIC pairs", Microelectronics Journal, vol. 41, no. 8, pp. 487-493, August 2010.
24 I. Voyiatzis, H. Antonopoulou, C. Efstathiou, "A Low-Cost Optimal Time Sic Pair Generator", Radioelectronics & Informatics, no. 4 (51), September–December 2010.
25 I. Voyiatzis, C. Efstathiou, H. Antonopoulou, A. Milidonis, "An Arithmetic Module-Based BIST Architecture for Two-Pattern Testing", IET Computers & Digital Techniques vol. 6, no 4, pp. 196-204, 2012.
26 I. Voyiatzis, C. Efstathiou, H. Antonopoulou, A. Milidonis, "An effective two-Pattern Test generator for Arithmetic BIST", Electrical and Computer Engineering vol. 39, no. 2, pp. 398-409, Feb. 2013.
27 C. Efstathiou, N. Moschopoulos, I. Voyiatzis, K. Pekmestzi, "On the design of modulo 2^n+1 dot product and generalized multiply-add units", Electrical and Computer Engineering vol. 39, no. 2, pp. 410-419, Feb. 2013.
28 C. Efstathiou, Z. Owda, G. Tsiatouhas, "New high speed multioutput carry look ahead adders", IEEE Trans. on Circuits and Systems II, vol. 60, no. 10. pp. 667-671, Oct. 2013
29 C. Efstathiou, N. Moschopoulos, N. Axelos, K. Pekmestzi, "Efficient modulo 2^n+1 multiply and multiply-add units based on modified Booth encoding", Integration the VLSI Journal, vol. 47, no. 1, pp. 140-147, Jan. 2014.

30 K. Tsoumanis, S. Xydis, C. Efstathiou, N. Moschopoulos, K Pekmestzi, "An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 4, pp. 1133-42, April 2014.

31 I. Voyiatzis, C. Efstathiou, "Input Vector Monitoring Concurrent BIST Architecture using SRAM Cells", vol. 22, no. 7, pp. 1925-29, IEEE Transactions on VLSI Systems, vol. 22, no. 7, pp. 1925-29, July 2014.

B2. In Conference Proceedings published as Books

1 K. Katzourakis, G. Kormentzas, K. Kontovasilis and C. Efstathiou, "A Virtual Signaling Protocol for Transparently Embedding Advanced Traffic Control and Resource Management Functionality in ATM Core Networks", Lecture Notes in Computer Science, pp. 259–271, vol. 2839, 2003.

C. In International Conference Proceedings

1 C. Efstathiou, C. Halatsis, "Modular realization of totally self-checking checkers for m-out-of-n codes", in Proceedings of the 13th IEEE International Symposium on Fault-Tolerant Computing, pp. 154-161, Milan, Italy, June 1983.

2 C. Efstathiou, C. Halatsis, "Modular design of totally self-checking checkers for 1-out-of-n codes", in Proceedings of the second GI/NTG/GMR Conference on Fault-Tolerant Computing Systems, pp. 164-176, Bonn, Germany, Sept. 1984.

3 T. Haniotakis, Y. Tsiatouhas, C. Efstathiou, D. Nikolos, "Novel Domino-CMOS Strongly Code Disjoint and Strongly Fault-Secure 1-out-of-3 and 2-out-of-3 Code Checkers", in Proc. of the 5th IEEE International On-Line Testing Workshop (IOLTW), pp. 174-178, Rodos, Greece, July 1999.

4 T. Haniotakis, Y. Tsiatouhas, D. Nikolos, C. Efstathiou, "On Testability of Multiple Precharged Domino Logic", in Proc. of the IEEE International Symposium on Quality of Electronic Design (ISQED'00), pp. 299-303, San Jose, California, March 2000.

5 C. Efstathiou, H. T. Vergos, "Modified Booth 1's complement and modulo 2^n-1 multipliers", in Proc. of 7th IEEE International Conference on Electronics, Circuits and Systems (ICECS), vol. II, pp. 637-640, Beirut, Lebanon, Dec. 2000.

6 H. T. Vergos D. Nikolos, M. Bellos, C. Efstathiou", A Formal Test Set for RNS Adders and an Efficient BIST Scheme", in Proc. of the 2nd IEEE Latin-American Testing Workshop (LATW), pp. 242-247, Cancun, Mexico, Feb. 2001.

7 H. T. Vergos, C. Efstathiou, D. Nikolos, "High-Speed Parallel-Prefix Modulo 2^n+1 Adders for Diminished-One Operands", in Proc. of the 15th IEEE Computer Arithmetic Symposium, 2001, pp. 211-217, Veil, Colorado, June 2001.

8 Y. Tsiatouhas, T. Haniotakis, D. Nikolos, C. Efstathiou, "Concurrent Detection of Temporary Faults Based on Current Monitoring", in Proc. of the IEEE International On-Line Testing Workshop, pp. 106-110, Taormina, Italy, June 2001.

9 C. Efstathiou, H. T. Vergos, D. Nikolos, "On the Design of modulo $2^n \pm 1$ adders", in Proc. of the 8th IEEE International Conference on Electronics, Circuits and Systems, (ICECS'01), vol. I, pp. 517-520, Malta, Sept. 2001.

10 C. Efstathiou, H. T. Vergos, D. Nikolos. "Ling Adders in CMOS standard cell technologies", in Proc.of the 9th IEEE International Conference on Electronics, Circuits and Systems, (ICECS), vol. II, pp. 485-488, Dubrovnik, Croatia, Sept. 2002.

11 C. Efstathiou, H. T. Vergos, D. Nikolos, "Fast Parallel–Prefix Modulo 2^n+1 Adders", 17th Conference on Design of Circuits and Integrated Systems (DCIS), pp. 65-70, Santander, Spain, Nov. 2002.

12 G. Dimitrakopoulos, H. T. Vergos, D. Nikolos, C. Efstathiou, "A Systematic methodology for Designing Area-Time Efficient Parallel-Prefix modulo 2^n-1 adders", IEEE International Symposium on Circuits and Systems (ISCAS) pp. vol. 5, 225-228, Thailand, Bangcoc, May 2003.

13 D. G. Nikolos, D. Nikolos, H. T. Vergos, C. Efstathiou, "Efficient BIST Schemes for RNS data paths", IEEE International Symposium on Circuits and Systems (ISCAS), vol. 5, pp. 573-576, Thailand, Bangcoc, May 2003.

14 G. Dimitrakopoulos, H. T. Vergos, D. Nikolos, C. Efstathiou, "A family of parallel-prefix modulo 2^n-1 adders", IEEE 14th International Conference on Application-specific Systems, Architectures and Processors (ASAP), pp. 326-336, Leiden, Netherlands, June 2003.

15 D. G. Nikolos, D. Nikolos, H. T. Vergos, C. Efstathiou, "An Efficient BIST scheme for High-Speed Adders", 9th IEEE International On-Line Testing Symposium" (IOLTS), pp. 89-93, Kos Island, Greece, July 2003.

16 C. Efstathiou, H. T. Vergos, G. Dimitrakopoulos, & D. Nikolos, "Efficient modulo 2^n+1 tree multipliers for diminished-1 operands", 10th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2003.

17 H. T. Vergos, C. Efstathiou, "Diminished-1 modulo 2^n+1 squarer design", 7th EuroMicro Conference on Digital System Design, (DSD), Rennes, France 2004.

18 N. Sklavos, C. Efstathiou, "On the FPGA Implementation of HAVAL Hash Function", EUROCON 2005, Serbia & Montenegro, Belgrade, Nov. 2005.

19 K. Katzourakis, G. Kormentzas, K. Kontovasilis and C. Efstathiou, "An Open Distributed Software System for Providing Traffic Control and Resource Management Functionality in Heterogeneous ATM Core Networks", Proceeding of the Fifth Int. Network Conference (INC2005), pp. 63 -72, Samos, Greece.

20 P. Souras, N. Sklavos, C. Efstathiou, and A. Rjoub, "Networks Security: Risk Management and Economics in Information Technology", Proc. of ACIT 2005, Jordan, Dec. 6-8, 2005.

21 G. Dimitrakopoulos, D. G. Nikolos, H. T. Vergos, D. Nikolos, C. Efstathiou, "New Architectures For Modulo 2^n-1 Adders", Proc. of ICECS 2005, Gammarth, Tunisia, Dec. 2005.

22 N. Sklavos, C. Efstathiou, "Area-Optimized Architecture & FPGA Implementation of the Pelican MAC Function", Proc. of the 2nd IEEE International Conference On Information and Communication Technologies, 2006, ICTTA '06

23 N. Sklavos, K. Touliou, C. Efstathiou, "Exploiting Cryptographic Architectures over Hardware Vs. Software Implementations: Advantages and Trade-Offs", Proc. of WSEAS Int. Conf. on AEE '06.

24 H. T. Vergos, C. Efstathiou, "Novel modulo 2^n+1 multipliers", 9th EUROMICRO Conference on Digital System Design (DSD'06), pp. 168-175, 2006.

25 I. Voyiatzis, C. Efstathiou "Two-pattern generation based on Accumulators with 1's Complement adders", In Proc. DTIS 2006.

26 H. T. Vergos and C. Efstathiou, "Efficient Modulo 2^k+1 Squarers", XXI Conference on Design of Circuits and Integrated Systems (DCIS), Barcelona, Spain, 22-24, Nov. 2006.
27 A. Kakarountas, H. Michail, C. Goutis and C. Efstathiou, "Implementation of HSSec: a High-Speed Cryptographic Co-processor", 12th IEEE Conference on Emerging Technologies and Factory Automation, Patras, Greece, Sept. 25-28, 2007.
28 N. Sklavos, C. Efstathiou, "SecurID Authenticator: On the Hardware Implementation Efficiency", Proc. of the 14th IEEE Int. Conf. on Electronics, Circuits and Systems (IEEE ICECS'07), Marrakech, Morocco, Dec. 11-14, 2007.
29 I. Voyiatzis, C. Efstathiou "An Efficient Architecture for Accumulator-Based Test Generation of SIC pairs", in Proc. of IEEE Int. Conf. on Design & Technology of Integrated Systems (DTIS 2008), Tozeur, Tunisia, March 26-28, 2008.
30 H. T. Vergos, D. Bakalis and C. Efstathiou, "Efficient Modulo 2^n+1 Multi-Operand Adders", Proc. of 15th IEEE International Conference on Electronics, Circuits & Systems (ICECS), pp. 694-697, Malta, August 31-September 3, 2008.
31 I. Voyiatzis, H. Antonopoulou, C. Efstathiou, "A Low-Cost Optimal Time SIC Pair Generator", Proc. of 6th IEEE East-West Design and Test Symposium (EWDT), Kiev, 2008.
32 C. Efstathiou, I. Voyiatzis, N. Sklavos, "On the modulo 2^n+1 multiplication for diminished-1 operands", Proc. of the 2nd IEEE Int. Conf. on Signals Circuits and Systems (SCS 2008), Tunisia, 7-11, Nov. 2008.
33 I. Voyiatzis, Antonopoulou H., C. Efstathiou, "Output Response Compaction in RAS-based Schemes", IEEE International Conference on Design & Technology ofIntegrated Systems in Nanoscale Technology (DTIS 2009), Cairo, Egypt, April 7-9, 2009.
34 C. Efstathiou, I. Voyiatzis, M. Prentakis, "Design methods for modulo 2^n+1 multiply-add units", Proc. of 7th IEEE East-West Design and Test Symposium (EWDTS), pp. 307-312, Moscow, Russia, Sept. 2009.
35 C Efstathiou, I. Voyiatzis, "Handling Zero in modulo 2^n+1 subtraction", Proc. of the 3nd IEEE Int. Conf. on Signals Circuits and Systems (SCS09), Tunis, Nov. 2009.
36 I. Voyiatzis, Th. Haniotakis, C. Efstathiou, H. Antonopoulou, A Concurrent BIST architecture based on Monitoring Square Windows, Proc. of IEEE Conference on Design & Techology in Nanoscale Era, (DTIS), Tunisia, 2010.
37 C. Efstathiou, I. Voyiatzis, "On the modulo 2^n+1 subtract units for weighted operands", Proc. of IEEE 22nd International Conference on Microelectronics (ICM), Cairo, Egypt, Dec. 2010.
38 C. Efstathiou, "Efficient modulo 2^n+1 subtractors for weighted operands", 17th IEEE International Conference on Circuits and Systems (ICECS) Athens, Greece Dec. 2010.
39 C. Efstathiou, I. Voyiatzis, "On the diminished-1 modulo 2^n+1 fused multiply-add units", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2011.
40 I. Voyiatzis, C. Efstathiou, H. Antonopoulou, "Low–overhead two dimensional two pattern test", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2011.

41 I. Voyiatzis, C. Efstathiou, H. Antonopoulou, "A Novel SRAM-Cell based Input Vector Monitoring Concurrent BIST architecture", Proc. of 16th IEEE European Test Symposium (ETS), May 2011.

42 C. Efstathiou, K. Pekmestzi, N. Axelos, "On the design of modulo 2^n+1 multipliers", 14th Euromicro Conference on Digital Systems Design (DSD), Sept. 2011.

43 I. Voyiatzis, C. Efstathiou, S. Hamdioui**,** C. Sgouropoulou, "ALU based address generation for RAMs", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2012.

44 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Test vector embedding in accumulators with stored carry in O(1) time", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2012.

45 I. Voyiatzis, C. Efstathiou, Y. Tsiatouhas, C. Sgouropoulou, "A novel architecture to reduce test time in march-based SRAM tests", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2012.

46 I. Voyiatzis, C. Efstathiou, D. Magos, C. Sgouropoulou, "Test set embedding into low-power sequences based on a traveling salesman problem formulation", Proc. of IEEE Conference on Design & Technology in Nanoscale Era, (DTIS), April 2012.

47 C**.** Efstathiou, N. Moschopoulos, C. Tsoumanis, C. Pekmestzi, "On the design of configurable modulo 2^n±1 residue generators", 15th Euromicro Conference on Digital Systems Design (DSD), Sept. 2012.

48 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Symmetric transparent online BIST for arrays of word-organized RAMs", DTIS 2013.

49 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Embedding test vectors in accumulator-based TPG using progressive search", DTIS 2013.

50 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "On line Testing of Logic and Memories in Emerging Technologies", ETS 2013.

51 K. Pekmestzi, C. Efstathiou, N. Moschopoulos, K. Tsoumanis, "Efficient modulo 2^n+1 multipliers for the IDEA block cipher", GLSVLSI, Paris, May 2013.

52 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, A Low-cost Input Vector Monitoring Concurrent BIST Scheme, IOLTS 2013.

53 K. Tsoumanis, C. Efstathiou, N. Moschopoulos, K. Pekmestzi, "On the Design of Modulo 2^n±1 Residue Generators", VLSI SOC, Istanbul, Oct. 2013.

54 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Transparent Testing for Intra-Word Memory faults", International Design and Test Symposium (IDT), Oct. 2013.

55 I. Voyiatzis, S. Neophytou, M. Michael, S. Hadjitheophanous, C. Sgouropoulou, C. Efstathiou, "Test set Embedding into Accumulator-generated sequences targeting Hard-To-detect faults", International Design and Test Symposium (IDT), Oct. 2013.

56 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Low Overhead Output Response Compaction in RAS Architectures", DTIS 2014.

57 I. Voyiatzis, C. Efstathiou, C. Sgouropoulou, "Accumulator-based Self-Adjusting Output Data Compression for Embedded Word-Organized DRAMs", DTIS 2014.

58 C. Efstathiou, K. Tsoumanis, K. Pekmestzi, I. Voyiatzis, "On the Design of Efficient Modulo 2^n+1 Multiply-Add-Add Units", DTIS 2014.

59 K. Tsoumanis, K. Pekmestzi, and C. Efstathiou, "Fused Modulo 2^n-1 Add-Multiply Unit", 21st IEEE International Conference on Electronics Circuits and Systems (ICECS), Marseille, France, 7-10 Dec. 2014.

60 N. Eftaxopoulos, G. Zervakis, K. Pekmestzi, C. Efstathiou, "High Performance MAC Designs", IDT 2014.

61 K. Tsoumanis, C. Efstathiou, K. Pekmestzi, "Modulo 2^n+1 Addition and Multiplication for Redundant Operands", IDT 2014.

62 I. Voyiatzis, D. Kavvadias, C. Sgouropoulou, C. Efstathiou, "Test set Embedding into Hardware generated sequences using an Embedding Algorithm", DTIS 2015

63 I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, "A Concurrent BIST Scheme for Read Only Memories", DTIS 2015.

64 I. Voyiatzis, C. Sgouropoulou, C. Efstathiou, "Detecting Untestable Hardware Trojan with Non-intrusive Concurrent On Line testing", DTIS 2015.

65 C. Efstathiou, K. Tsoumanis, K. Pekmestzi, I. Voyiatzis, "Modulo 2^n+1 Fused Add-Multiply Units", IS VLSI 2015.

66 K. Pekmestzi, K. Tsoumanis, C. Efstathiou, "Fused Modulo 2^n+1 Add-Multiply unit For Weighted Operands", DTIS 2016.

67 K. Tsoumanis, K. Pekmestzi, C. Efstathiou, "Fused Modulo 2^n+1 Add-Multiply unit for Diminished-1 Operands", MOCAST 2016.

NC. In National Conference Proceedings

1 D. Kavadias, S. Sinitos, I. Voyiatzis, H. Antonopoulou, C. Efstathiou, "On Embedding Test Sets into Hardware Generated Sequences", in Proceedings of IEEE Panhellenic Conference on Informatics (PCI), Greece, September 2010.

2 I. Voyiatzis**,** K. Axiotis, N. Papaspyrou, H. Antonopoulou, C. Efstathiou, "Test Set Embedding Into Low-power BIST Sequences using Maximum Bipartite Matching", in the 16th Panhellenic Conference on Informatics, PCI 2012.

3 I. Nikopoulos, A. Milidonis, C. Efstathiou, C. Sgouropoulou, I. Voyiatzis, "Stealth Assessment of Hardware Trojans in simple Processors" in the ACM proceedings of PCI 2014.

4 I. Voyiatzis and C. Efstathiou, "Accumulator-based Generation for Serial TPG", 19th Panhellenic Conference on Informatics (PCI) 2015.

5 I. Voyiatzis and C. Efstathiou, "On the use of hard faults to generate test sets", 19th Panhellenic Conference on Informatics (PCI) 2015.

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LECTURE NOTES

1. Computer Architecture and Organization
2. Advanced Computer Architectures and Multimedia Systems
3. Data Communications and Computer Networks
4. Microprocessors and Microcomputers
5. Open Embedded Hardware/Software Development Systems (Arduino, Raspberry).